Discrete Domain Switching in Scaled Oxide-Channel Ferroelectric FETs

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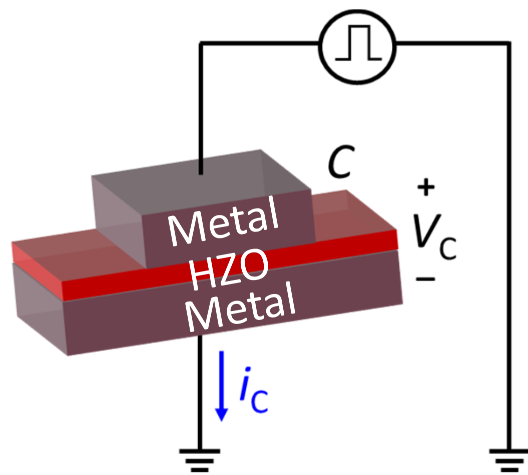
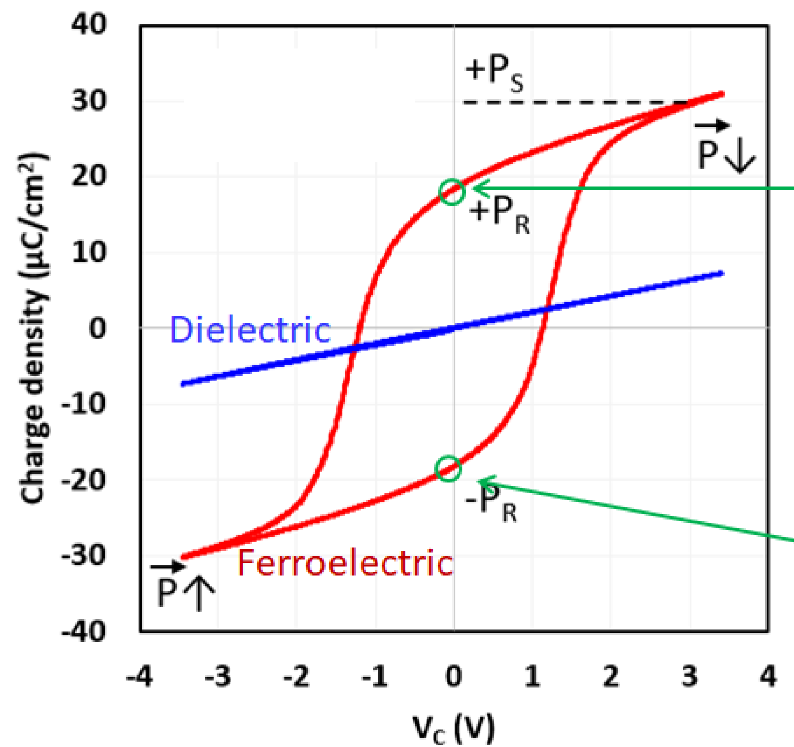
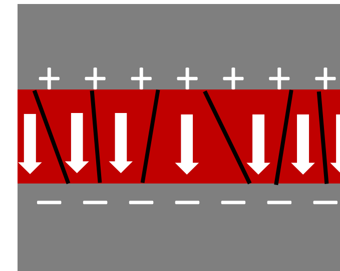
Ferroelectric $Hf_xZr_{1-x}O$

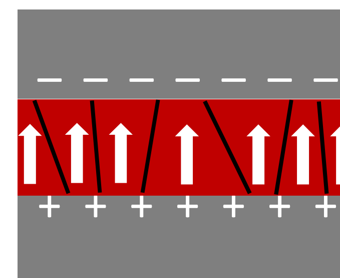
Ferroelectric (FE) $Hf_xZr_{1-x}O$ (HZO):

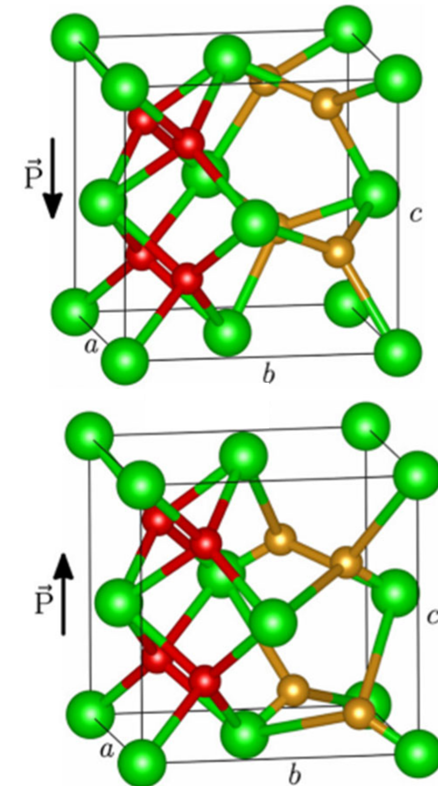
- stores polarization charge due to unique crystal structure
- CMOS compatible









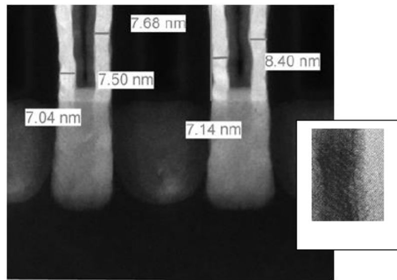


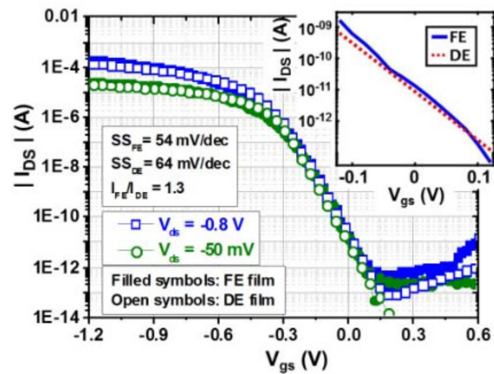
● : Hf/Zr atom ● : O atom ● : O atom for ferroelectricity

Materlik, JAP 2015

Integration of FE-HZO on CMOS: from FEOL to BEOL

Logic

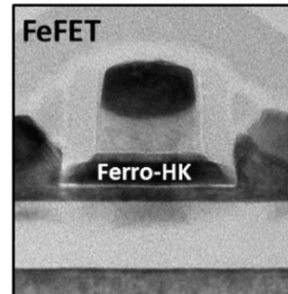


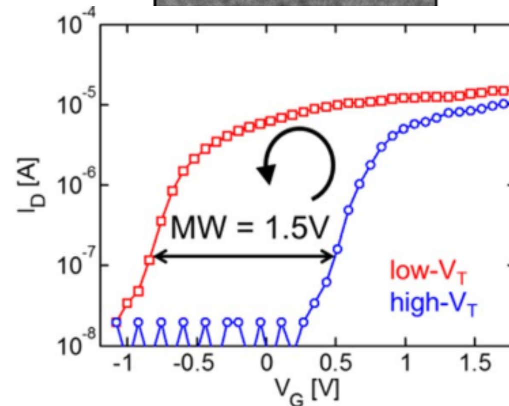


FE-FinFET

Krivokapic, IEDM 2017

Memory

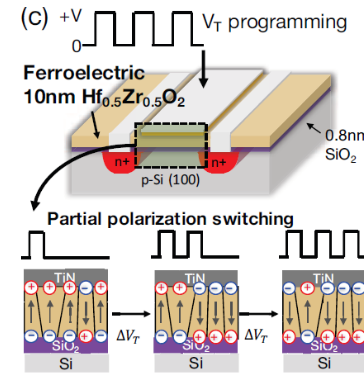


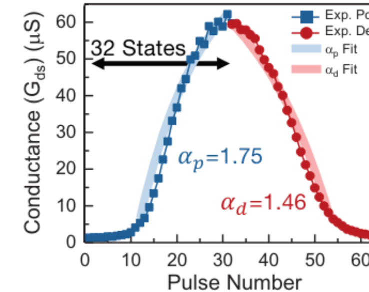


FE-FET

Dunkel, IEDM 2017

AI hardware

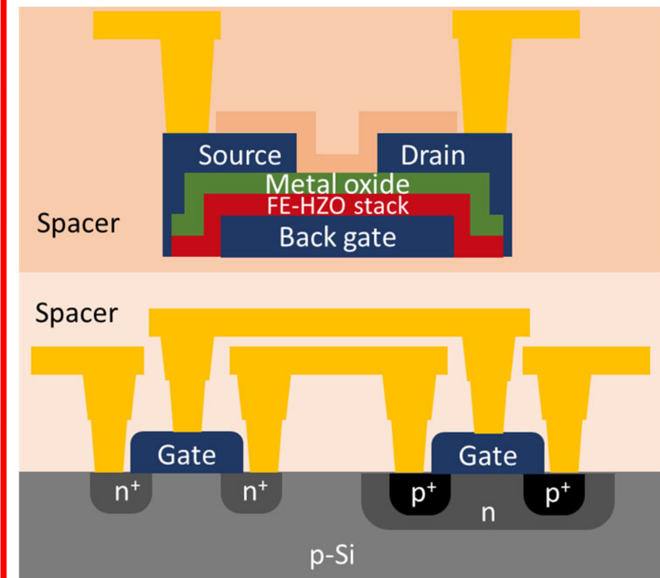




FE Analog Synapse

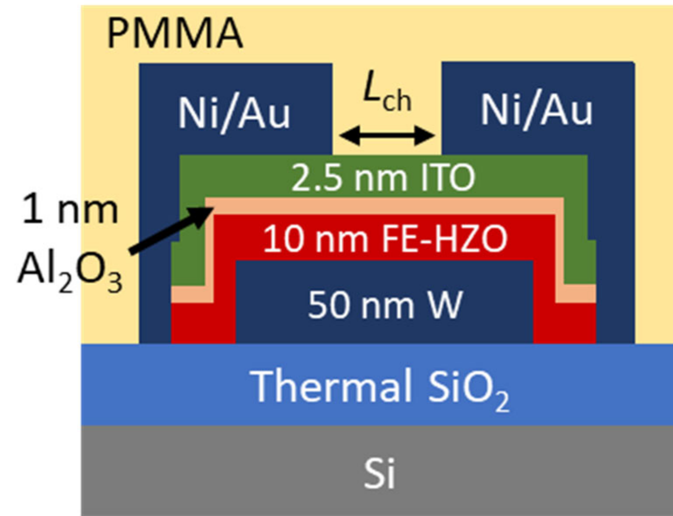
Jerry, IEDM 2017

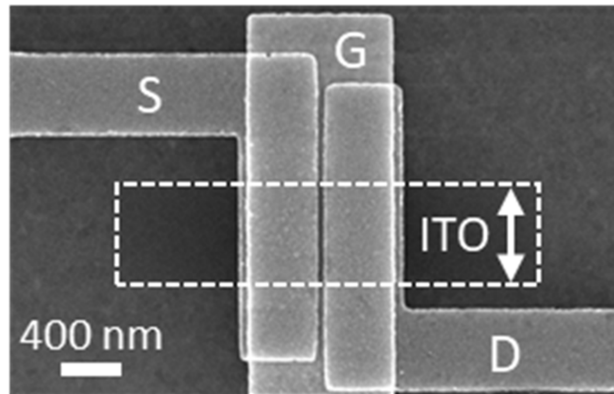
BEOL FE technology

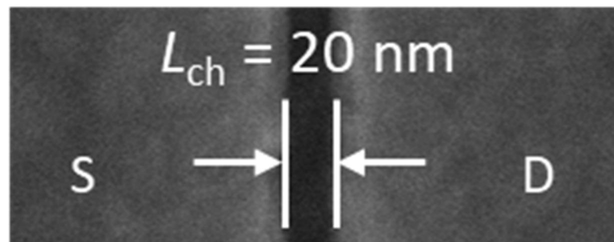


Our focus: BEOL-compatible FE-FET technology for memory and AI applications

Design and fabrication of BEOL FE-FETs







- 50 nm W sputtering
- W back gate patterning
- 10nm HZO/1nm Al_2O_3 by PEALD
- RTA @ T = 400 °C, 1 min
- Gate via opening
- ITO sputtering
- Mesa patterning
- Ni/Au contact deposition
- Probe-pad fabrication

- CMOS-compatible thermal budget
- Highly-scaled device geometry

Working principle of FE-FETs

Drain current, log I_d

"Erase"

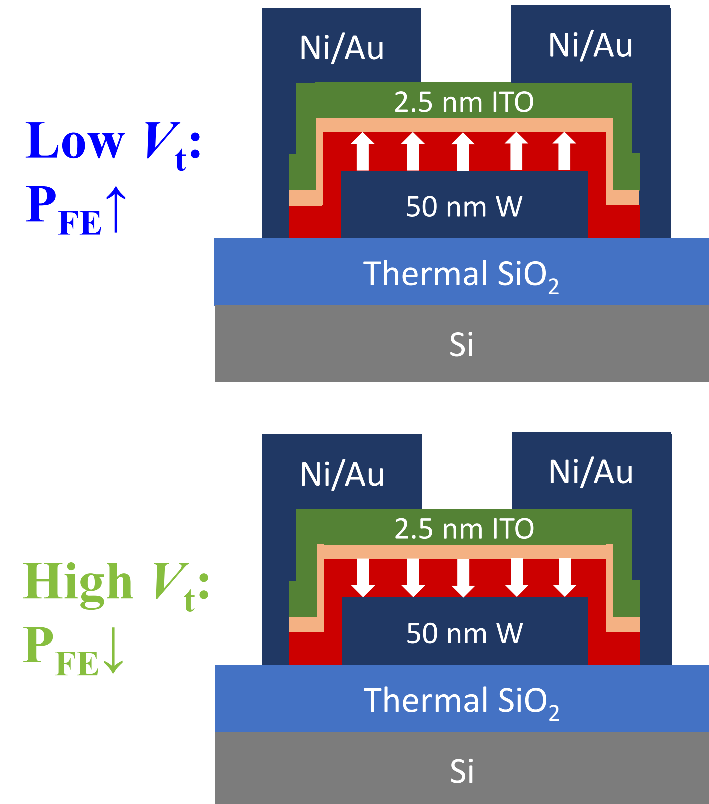
Low V_t

"Program"

Memory window (MW) defined @1 µA/µm

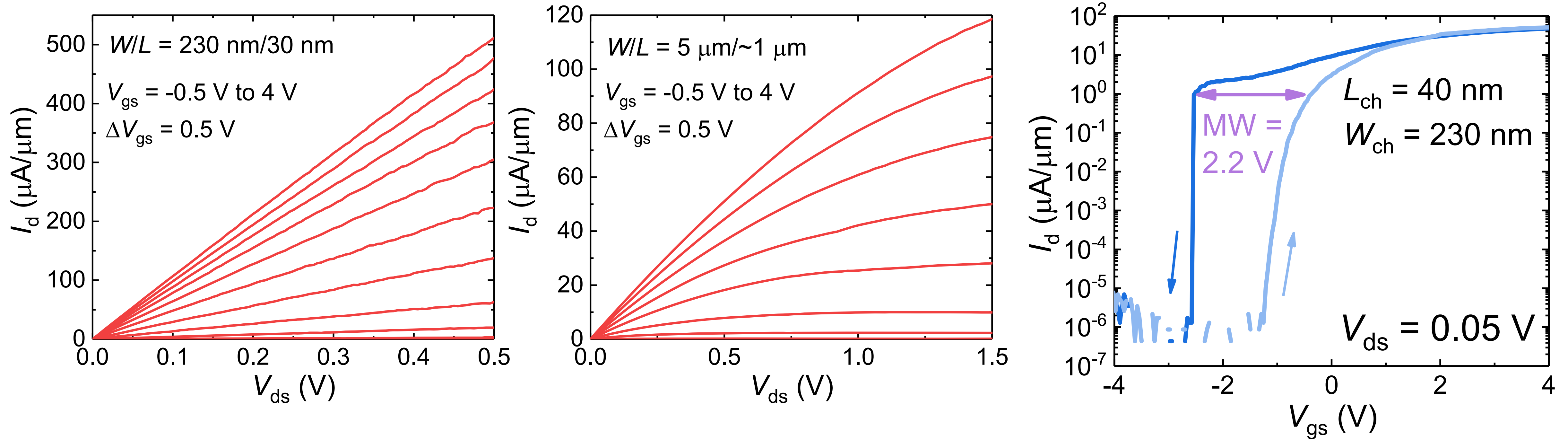
High V_t

Gate voltage, V_{gs}



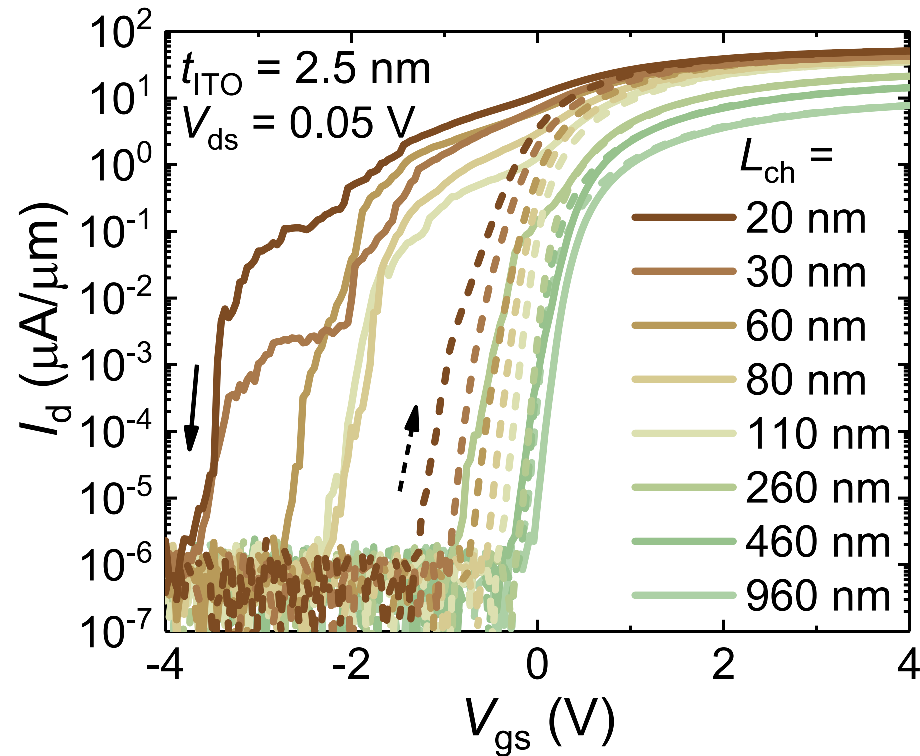
- Two V_T states with complete FE polarization switching

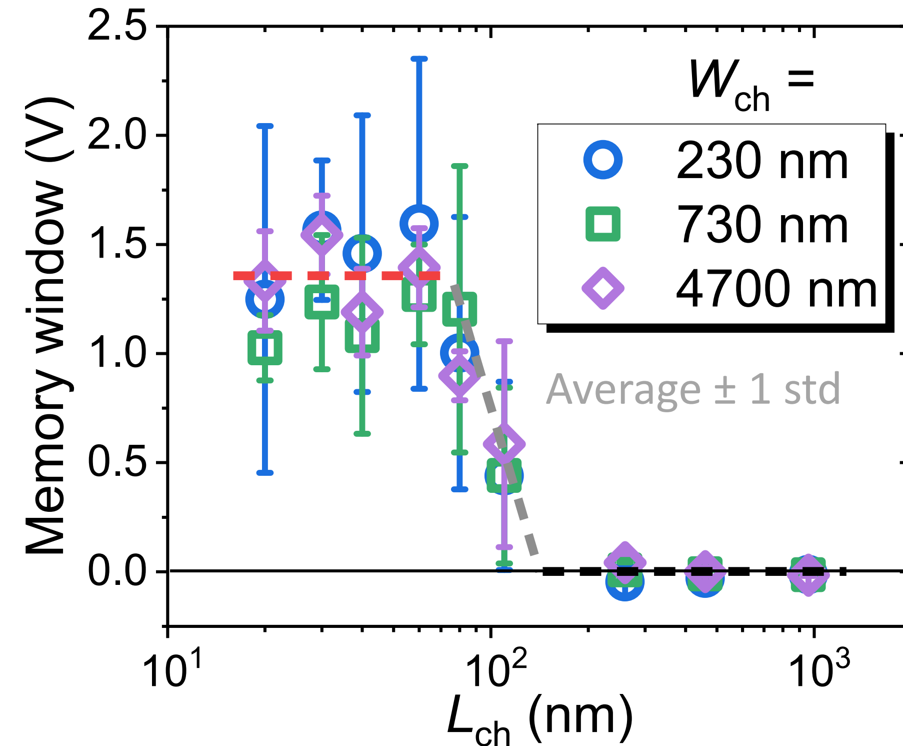
DC I-V characteristics of FE-FETs



- Linear turn-on and high on-state current
- Prominent counter-clockwise FE memory behavior
- Large MW = 2.2 V @ L_{ch} = 40 nm

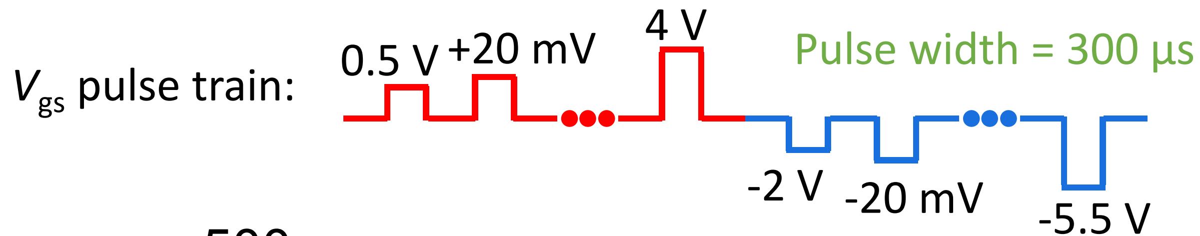
Impact of L_{ch} scaling on MW



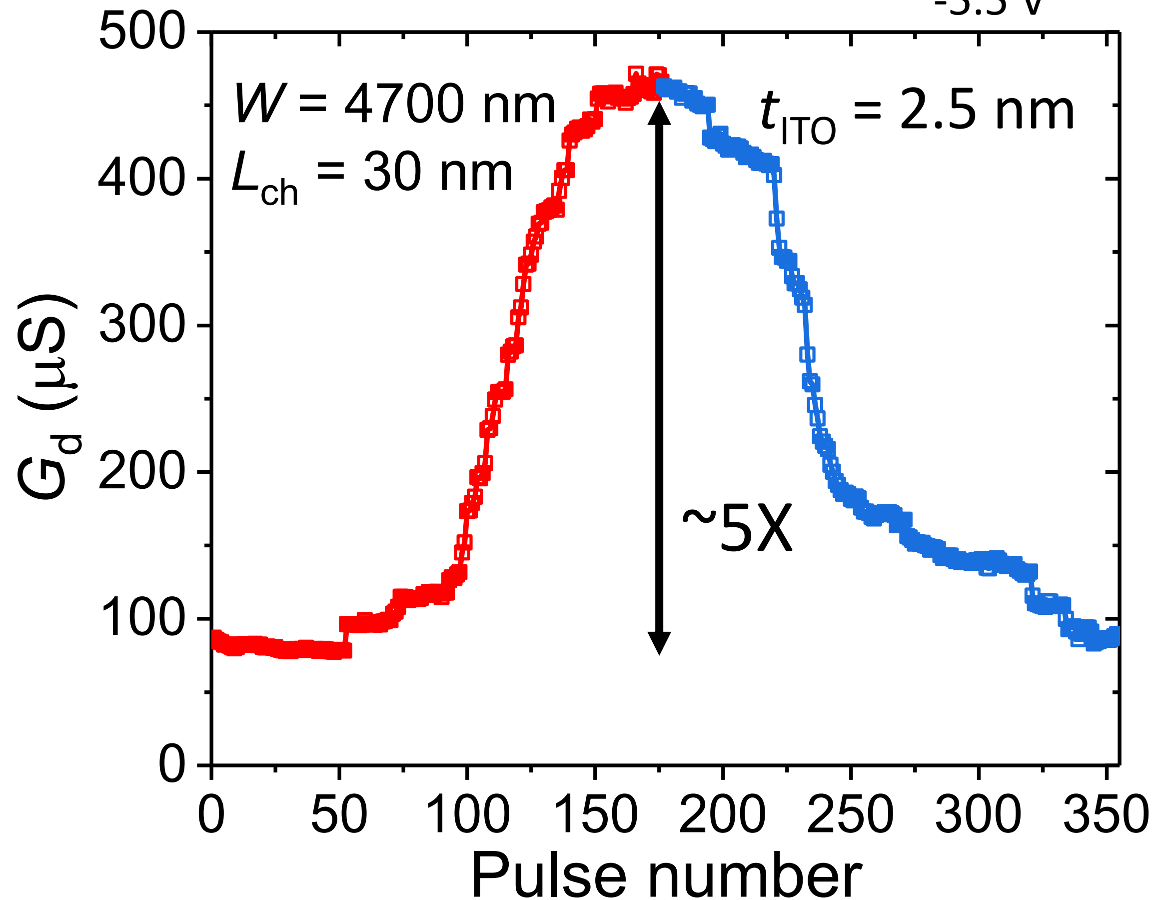


- Saturated MW vs. L_{ch} when L_{ch} < 80 nm
- Sharp decrease of MW when L_{ch} > 80 nm
- MW rather independent of channel width

Gradual conductance switching: artificial synapses

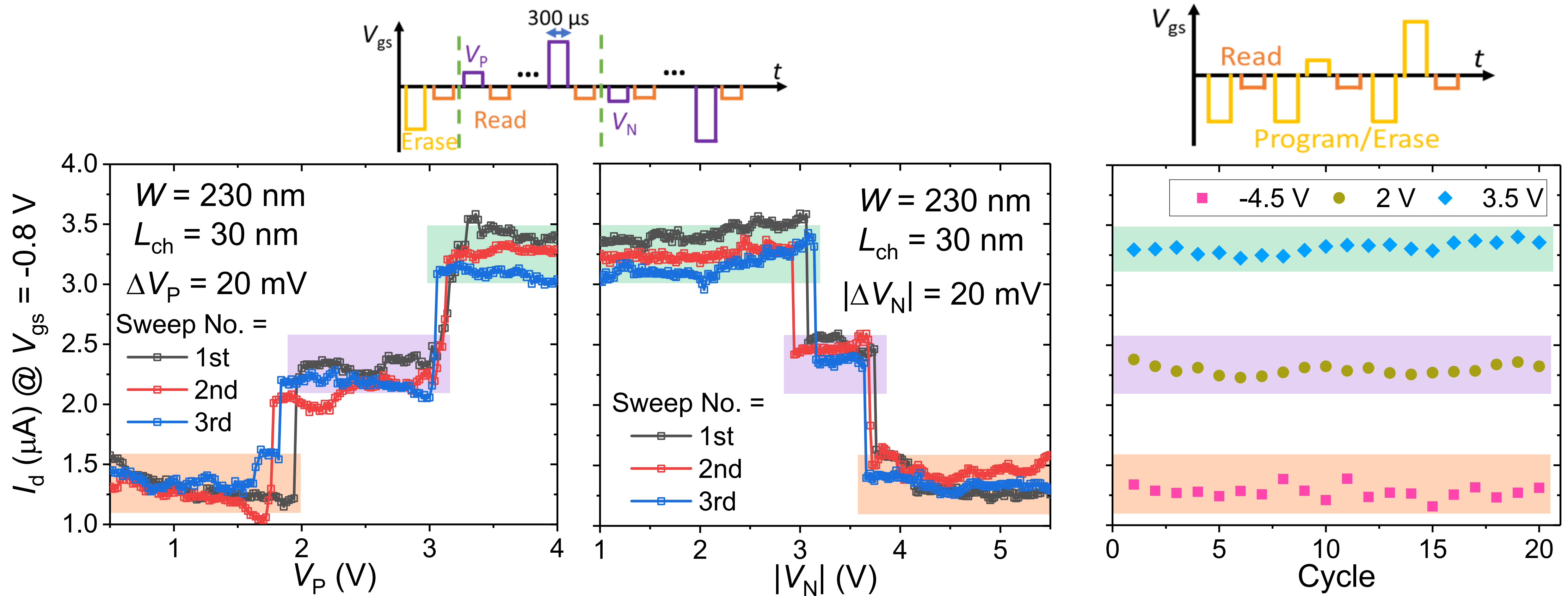


Read after each pulse @ V_{ds} = 0.05 V, V_{gs} = -0.8 V



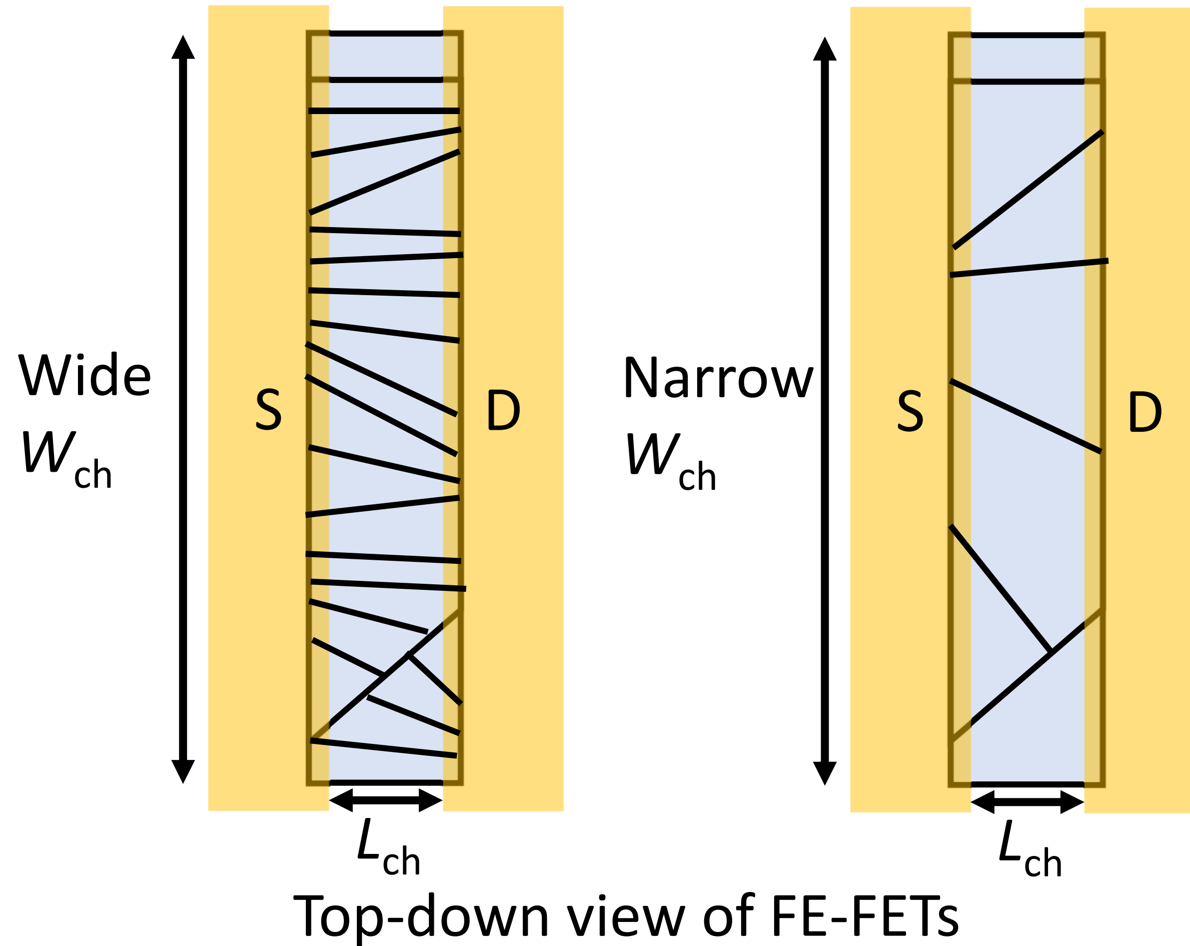
- Wide channel ~5 µm
- Conductance dynamic range ~5x
- Overall symmetric modulation

Discrete conductance switching: multi-state memory



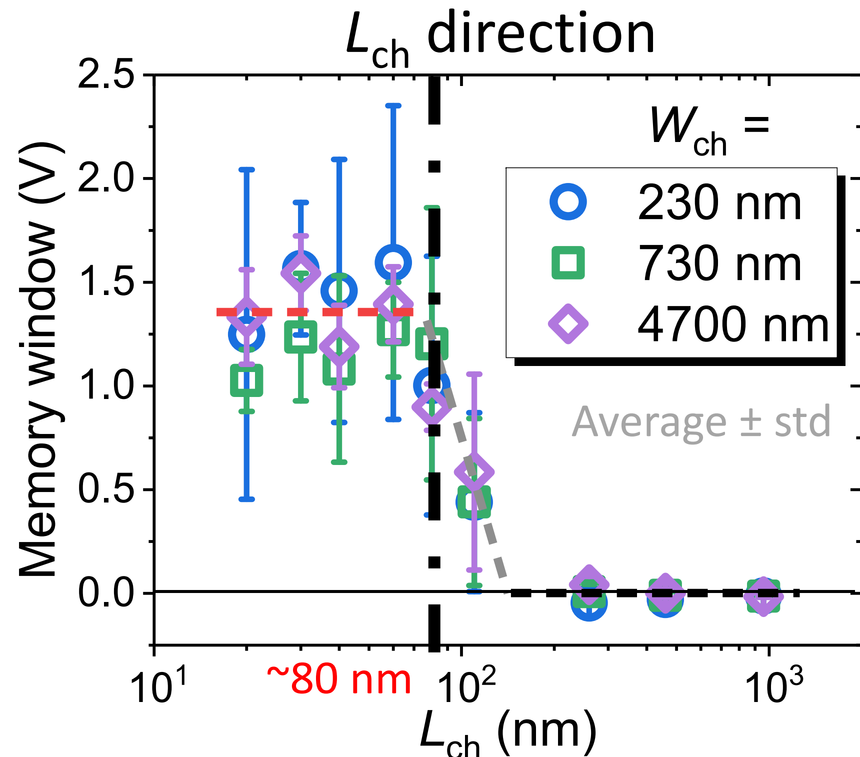
- Narrow channel = 230 nm
- 3 distinct conductance states
- Discrete switching seen in highly-scaled devices (both W_{ch} and L_{ch})

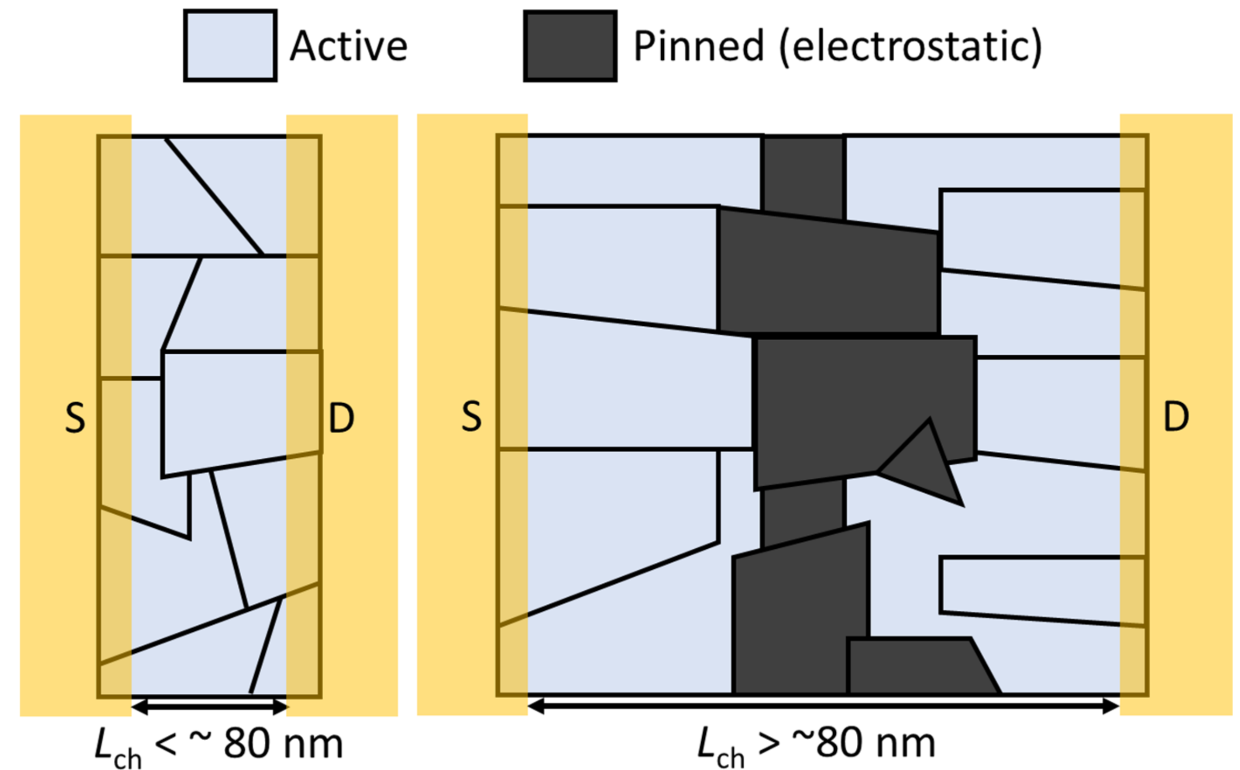
Discrete domain switching



- Discrete local activation fields (E_a) for different domains
- Wider devices → smoother distribution of local activation field

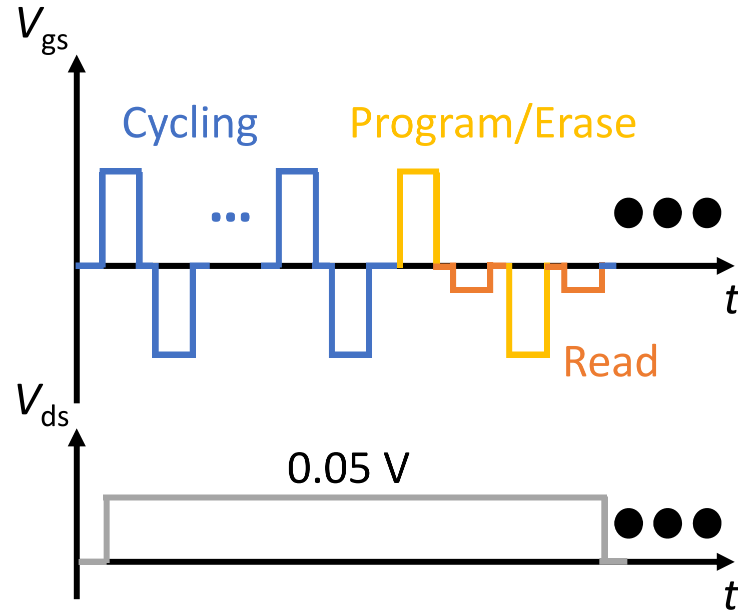
An interesting question: what is the domain size?

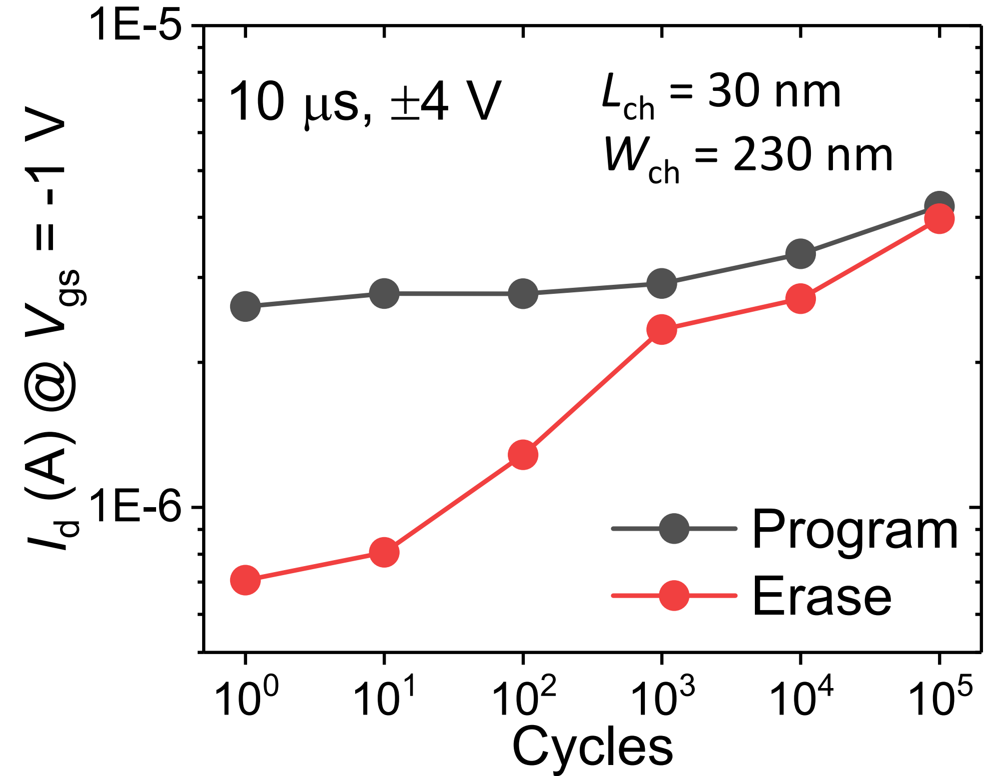




- Wide E_g > 3 eV for ITO → weak vertical E-field in the off state in the channel
- Switching of FE polarization in a domain likely requires direct contact to S/D
- Domain size estimated to be ~40 nm

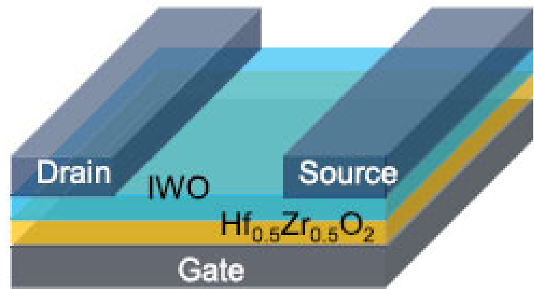
Endurance characteristics





- Endurance ~10^5 cycles
- Clear increase of current in "Erase" state with more cycling

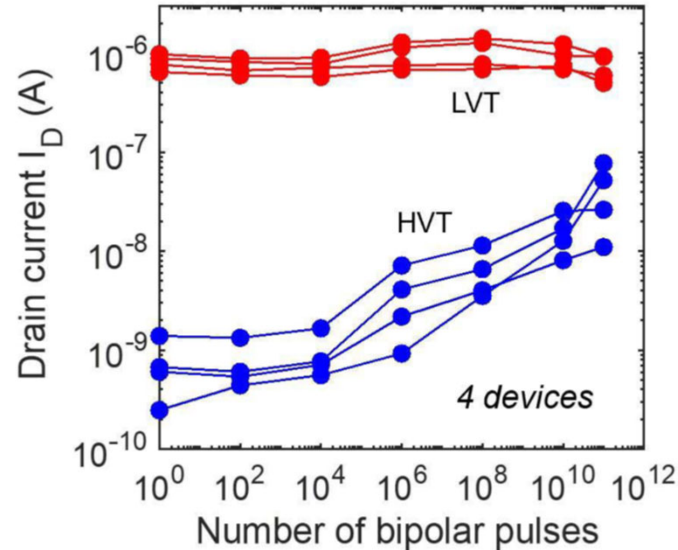
Endurance characteristics in the literature



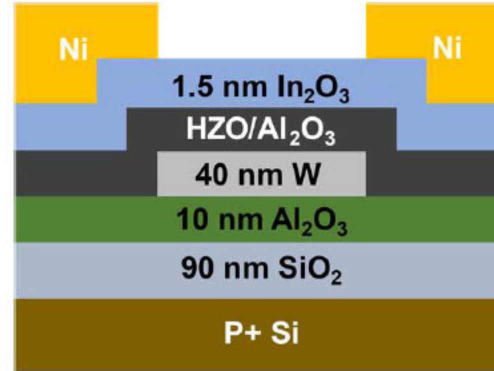
5 nm HZO

IWO channel

W_{ch} = 126 nm



Dutta, EDL 2022

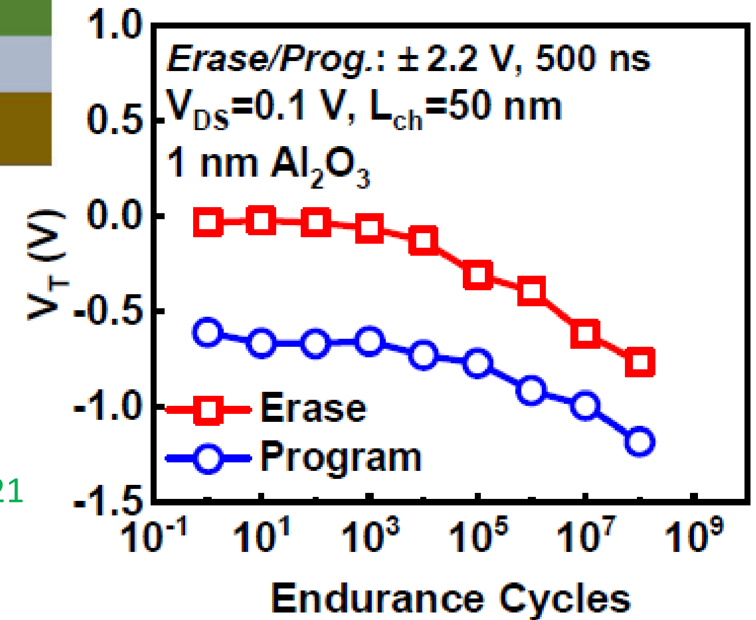


8 nm HZO/
1 nm Al_2O_3

In_2O_3 channel

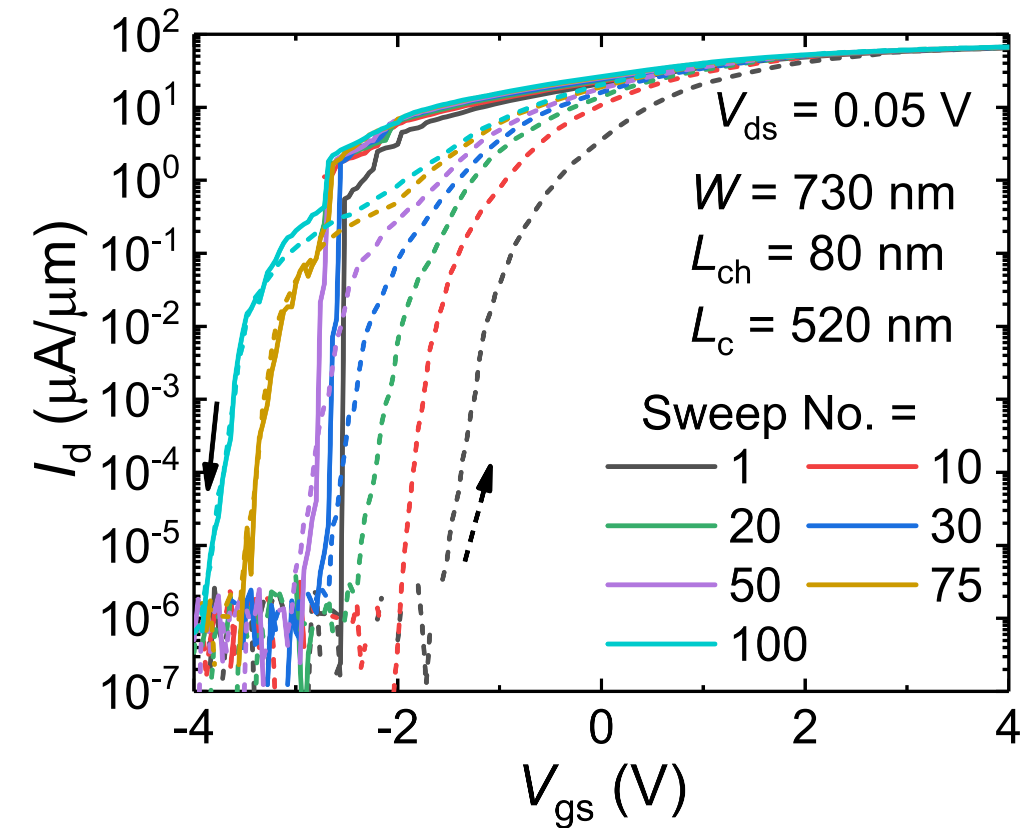
Lin, IEDM 2021

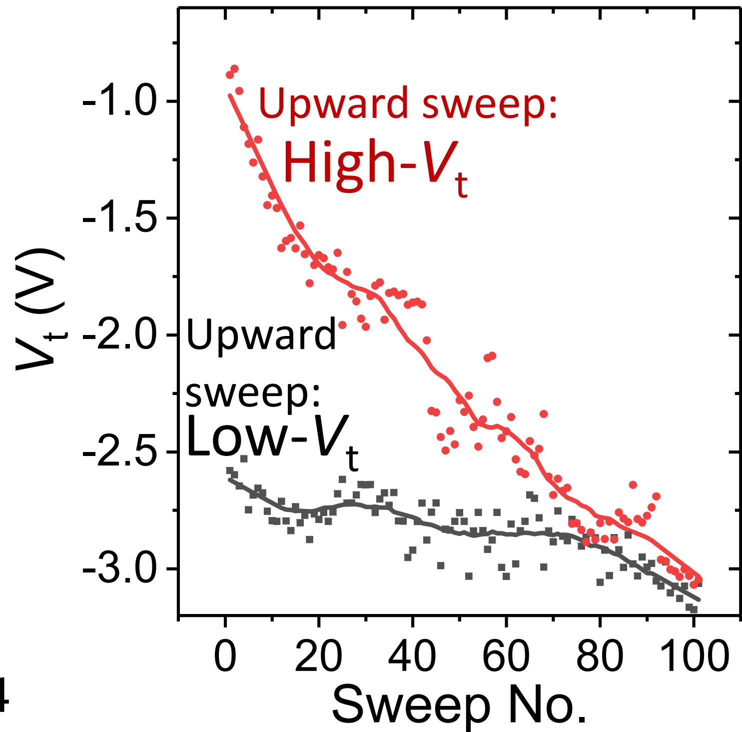
W_{ch} ~ 2 um (?)

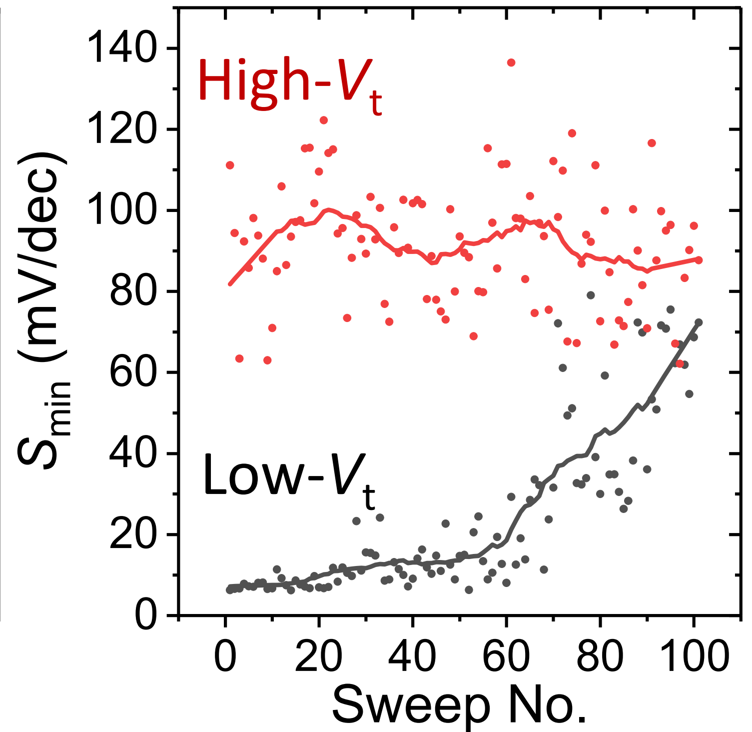


- Negative V_t shift commonly seen in oxide-channel FE-TFTs
- Origin of this?

Understanding endurance: V_t and S shift



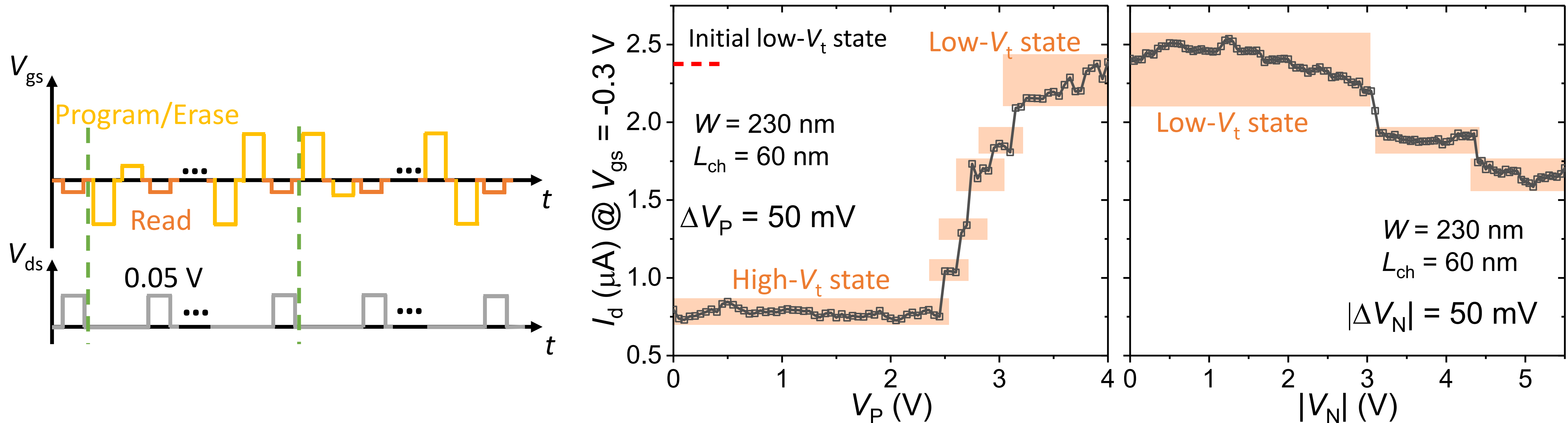




Minimum S defined within a current range that is at least one decade

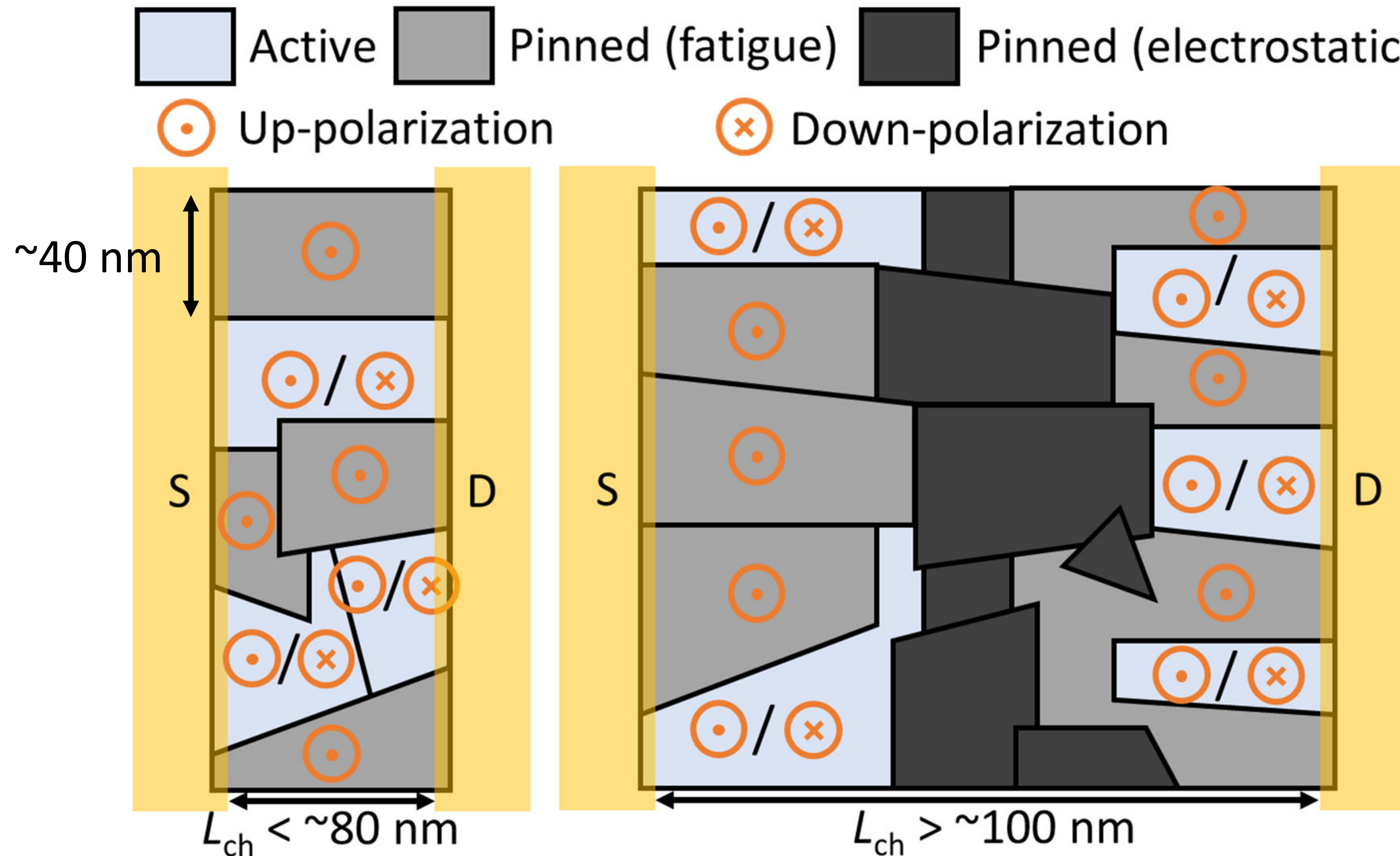
- Upward sweep: $\Delta V_t < 0$, S unchanged → no interface state generation
- Downward sweep: V_t nearly unchanged

Understanding endurance: domain pinning



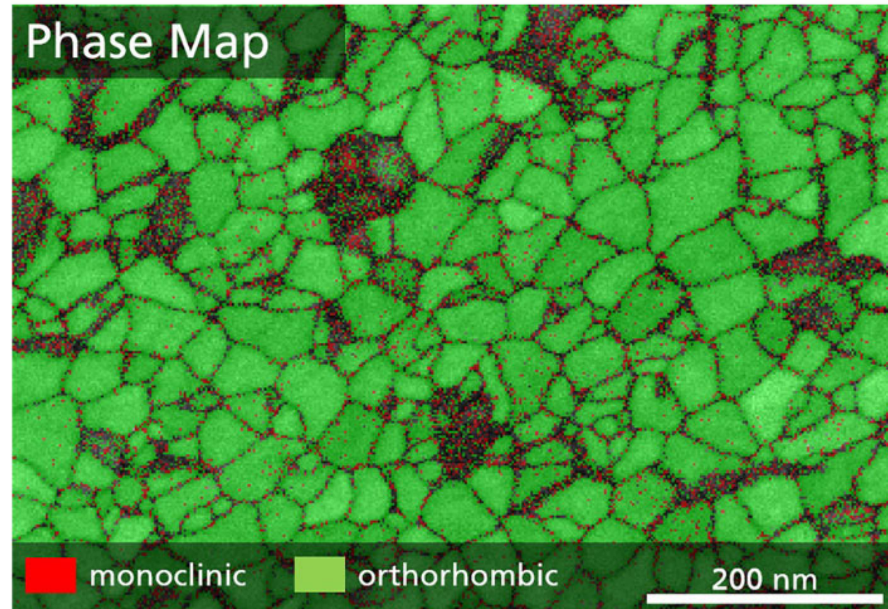
- Virgin narrow-channel device (no endurance cycling)
- Conductance not going back to original value after full cycle
- Pinning of certain FE domains in low-V_t state ("up" direction)
- Origin of oxide-channel FE-FET fatigue?

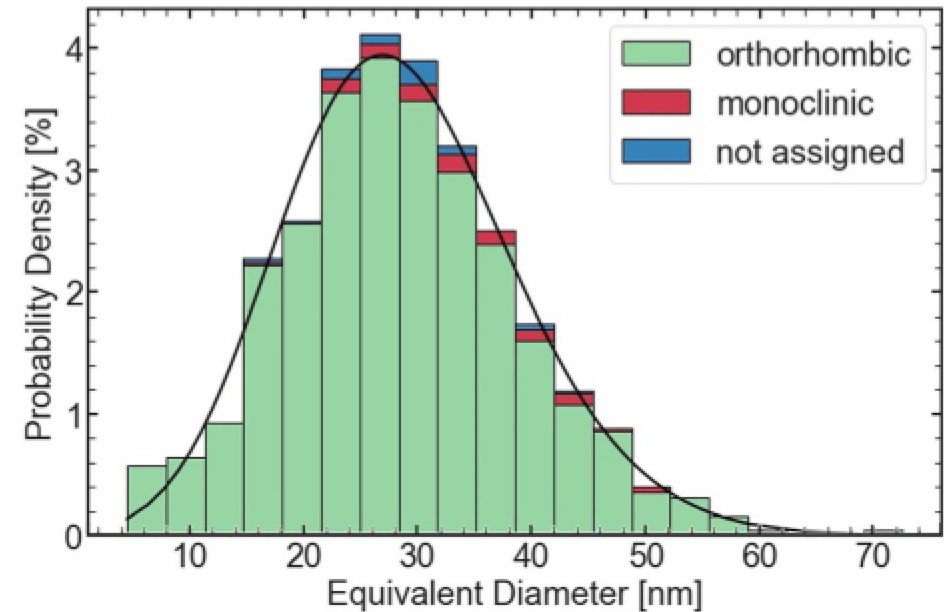
Hypothesis on domain switching and pinning



- Domains can be pinned due to fatigue or due to electrostatically inactive

Possible origin of domain structures





Lederer, APL 2019

- Polycrystalline nature of HZO film
- Grain size ~ 20-40 nm, close to our estimated domain size

Conclusions

- Rich functionality of FE-HZO for BEOL applications
- Large MW requires L_{ch} < ~80 nm, while MW independent of W_{ch}
- Discrete domain switching observed in narrow-width oxide-channel FE-FETs
- FE-FET fatigue arises from negative V_t shift and domain pinning

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